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TECHNICAL OPERATING REPORT ON THE DATA INTEGRATION AND COLLECTION ENVIRONMENT (DICE) INSTRUMENTATION SYSTEM DESIGN

TRW
293 Highway 247, South
Warner Robins, Georgia 31088

June 1992

Interim Report for Period May 1991 to May 1992

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Avionics Directorate
Wright Laboratory
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433-6543

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Current and planned avionics radar systems are highly sophisticated in their capabilities and heavily dependent on Embedded Computer Systems (ECS) for their operation. Avionics radar systems containing ECS provide a high level of flexibility in both system configuration and capability. However, increased flexibility requires increased logistical support. This support includes both hardware and software maintenance. Air Force Logistics Command (AFLC) is conducting a concentrated effort to limit the rising cost of ECS support while responding to user requests for improving these systems. This effort and the ECS Support Improvement Program (ESIP), a program implemented to address the problem of developing a rapid turnaround capability for airborne avionics radar systems, have as one of their research and development objectives to develop the necessary rapid turnaround capabilities to support mission critical ECS. Rapid Turnaround (RT) is defined as correcting a system deficiency in a timely fashion through some combination of software, firmware, and/or hardware modifications. The RT concept evolved from the overall AFLC objective to decrease the time and resources required to implement operational or maintenance changes in deployed ECS.

Avionics systems are designed with internal data buses which can provide access to vast amounts of data. The data buses contain data, such as MIL-STD-1553 and H009 and are located primarily in the programmable signal processor.

The need for an instrumentation system hosted on-board a tactical aircraft resulted in the development of the Data Integration & Collection Environment (DICE) System by TRW and the Air Force. The Dice System is being designed to collect and record radar data during tactical missions to aid radar analysts in determining radar system deficiencies and anomalies.

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1 SCOPE

1.1 Identification

This Technical Operating Report (TOR), prepared in accordance with DI-S-30559/T, describes the instrumentation system design (ISD) identified as the Data Integration and Collection Environment (DICE) system. This report includes the top level and intermediate level hardware design information.

1.2 Background

The joint AFLC/AFSC Embedded Computer Resources Support Improvement Program (ESIP) is tasked to provide a means of providing reliable rapid radar system reprogramming capability. This capability will provide a means to perform software enhancements on current and future radar systems with significant reconfiguration of all fielded units within days. TRW's task is to develop a laboratory prototype of an on-board instrumentation system which is capable of collecting the useful data from the avionics radar system. The data collected by this system will aid analyst to perform reprogramming in a meaningful manner. The F-15 APG-63 radar is the initial target for this system.

1.3 Document Overview

This TOR provides the top level and intermediate level hardware design of the DICE system. This report is structured in the following manner:

1) Section 1 presents a brief description of the overall objectives of this system.

2) Section 2 identifies the applicable documents, both Government and non-Government, for the DICE system.

3) Section 3 presents the instrumentation system design

4) Section 4 provides general information that aids in understanding this document (e.g., a list of acronyms and other abbreviations used herein).

2 REFERENCED DOCUMENTS

The following documents of the exact issue shown form a part of this document to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this document, the contents of this document shall be considered a superseding requirement.

Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the contracting agency or as directed by the contracting officer.

2.1 Government Documents

SPECIFICATIONS:

DI-S-30559/T 12 May 1989	Data Item Description, Technical Operating Report
MIL-E-5400T 16 November 1979.	Electronic Equipment, Aerospace General Specification

STANDARDS:

MIL-STD-461C 04 August 1986	Electromagnetic Emission And Susceptibility Requirements For The Control Of Electromagnetic Interference
MIL-STD-462 31 July 1967.	Electromagnetic Interference Characteristics, Measurement of
MIL-STD-810E 14 July 1989	Environmental Test Methods And Guidelines
MIL-STD-1472D 14 March 1989	Human Engineering Design Criteria For Military Systems Equipment And Facilities
MIL-STD-1553B 21 September 1978	Aircraft Internal Time Division Command/Response Multiplex Data Bus
MIL-STD-1788A 31 July 1989	Avionics Interface Design Standard
MIL-STD-2036 June 1991	General Requirements For Electronic Equipment Specifications (COTS and Ruggedized Equipment Applications And Testing)

DRAWINGS:

NONE

OTHER PUBLICATIONS:

NONE

2.2 Non-Government Documents

SPECIFICATIONS:

7 May 1980	F-15 Instrumentation Interface Unit (IIU) Specification, Hughes Aircraft Corp.
H-009 12 March 1969	Multiplexer Bus System Specification, Mc Donnell Douglas Aircraft Corp.

STANDARDS:

None

DRAWINGS:

None

OTHER PUBLICATIONS:

F33615-87-C-1538	Radar Readiness Technology Report, Warner Robins Air Logistics Center
	Radstone CPU3A Technical Specification, Radstone Corp.
	MIL-STD-1553B Monitor System, SBS
3173914-100	Programmable Signal Processor (PSP) Reference Manual
SD171500009-01 30 June 1989	Airborne Instrumentation Interface Unit System Manual, Comptek Research Inc.

3 DICE SYSTEM DESIGN

3.1 Design Criteria

The following paragraphs describe the design criteria for the basic laboratory prototype of the DICE system. The smart record and flight version options are not addressed in this document.

3.1.1 Design Objectives

The DICE system is designed to meet or exceed the following criteria:

1) Provide the capability to configure and control the collection of specific APG-63 radar and weapon systems data.

2) Provide for the collection of any and all D-Bus, PMUX, CCMUX, and PACS communication data.

3) Provide a data storage capability which exceeds two hours.

4) Provide a mechanism for replaying the recorded data to the instrumentation data reduction and analysis system (IDRAS) in a time phased manner.

5) Identify source for dual compatible militarized and commercial-off-the-shelf components (COTS).

6) Provide prototype road map for the system for production.

7) Provide for growth in filtered data capture processing, throughput, and data storage capacity.

3.1.2 System Definition

The laboratory DICE system is a Motorola 68030 30 MHz, VME based system utilizing a custom programmable hardware interface which operates under the control of operational software written in Ada. The system uses the commercial version of the RADSTONE CPU3A militarized processor. The data storage system consists of the EXABYTE EXB-8500 8mm cartridge tape system. The programmable hardware interface design utilizes Xilinx field programmable gate array (FPGA) logic. Figure 3-1 provides a top level view of the laboratory DICE system.

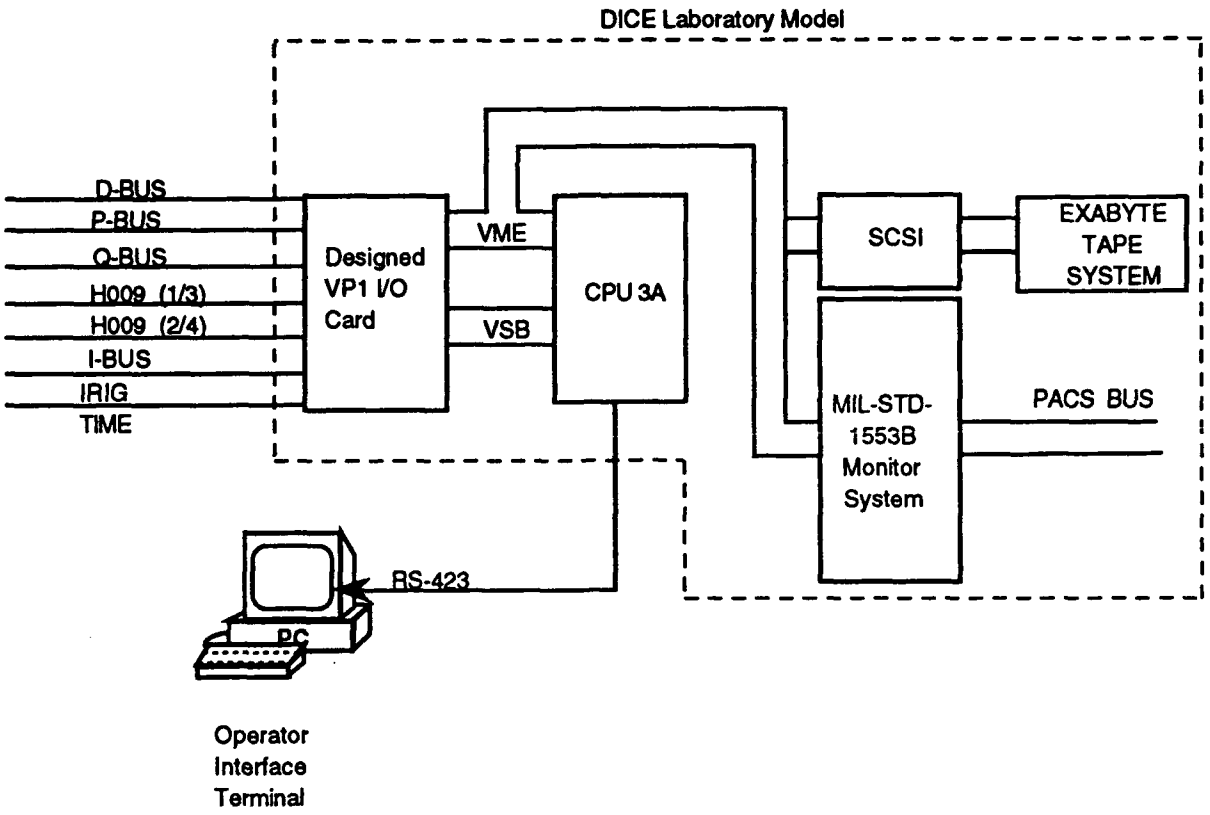

Figure 3-1. DICE Laboratory System Diagram

3.1.3 Data Volumes and Rates

After laboratory level analysis of the target systems medium pulse repetition frequency (MPRF) Track Mode data transmissions, the following data rates and volumes have been established as a minimum load capability for the DICE system.

Table 3-1. Data Volume and Rate Criteria

SOURCE	WORD COUNT	WORD SIZE(bytes)	TRANSMISSION RATES(Hz)	VOLUME (Bytes/Sec)
D-BUS	1024	3072	97.7	300,134
P-BUS	16	48	97.7	4,690
Q-BUS	16	48	97.7	4,690
I-BUS	15	45	97.7	4,396
H009 1/3	211	422	20.0	8,440
H009 2/4	283	596	20.0	11,320
Total Volume Rate				333,670

The DICE system has an initial throughput rate of 1 Mbyte/sec. Based on the target systems data rates and volume, the DICE system has a capacity utilization of 34% with the remaining 65% available for future growth. The DICE system is designed with flexibility and growth in mind. The hardware

design allows for technology insertion and easier system retargetting. The data storage and data transfer capacity can be increased by incorporating enhanced versions of the current components [1]. The software for the basic system utilizes less than 20% of the available processor resources providing adequate growth for future needs.

3.2 Hardware Design

3.2.1 Interface Control Design

3.2.1.1 Timing Diagrams

Figure 3-2 represents target system waveforms that are to be recorded and played back in the laboratory. Figure 3-3 represents the D-Bus data synchronization and blocking scheme. Figure 3-4 depicts the PCM waveforms of the target system. Figure 3-5 represents the inter-range instrumentation group (IRIG) B time code format.

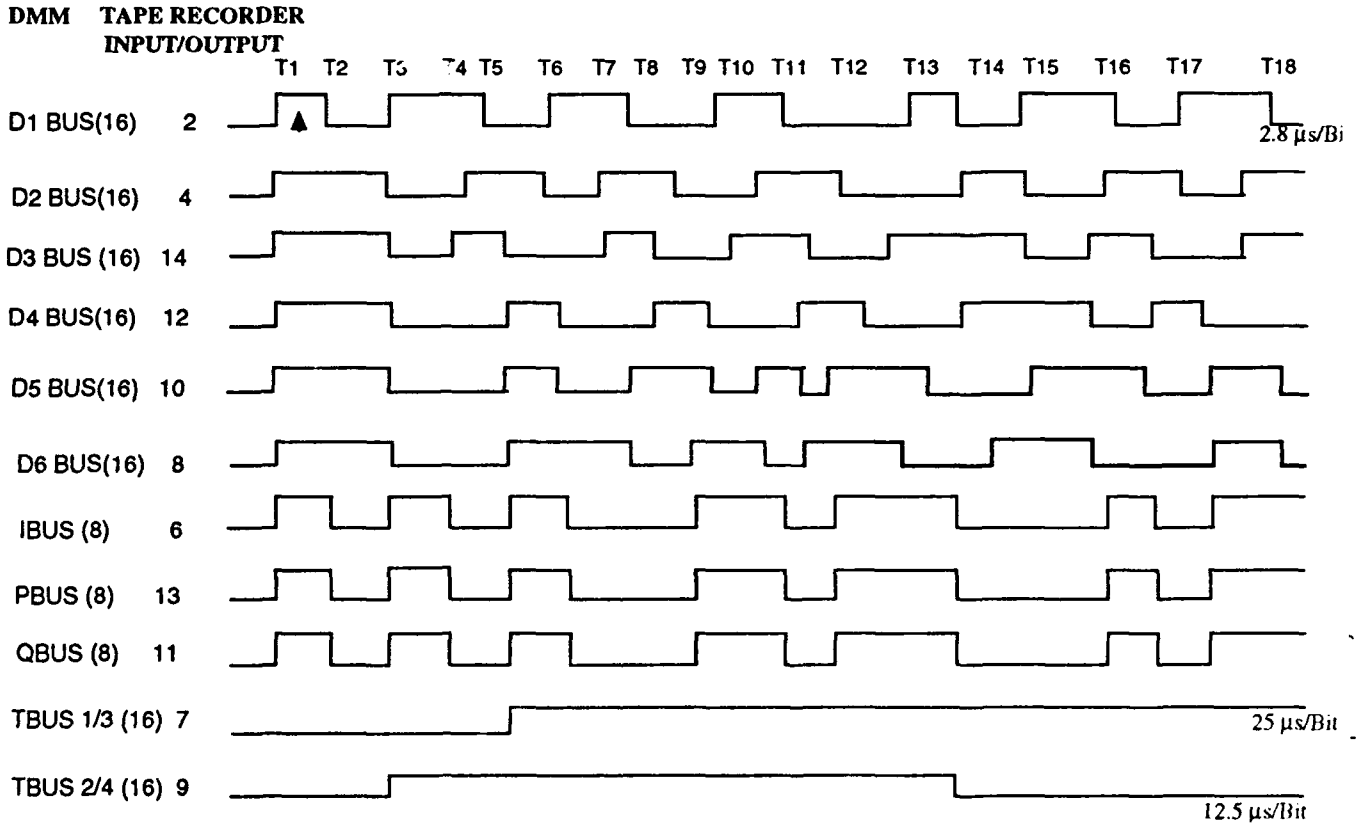

Figure 3-2. Target System Waveform Timing Diagram

[1] The enhanced versions of these components (tape unit and interface system) will not be available until mid-1993.

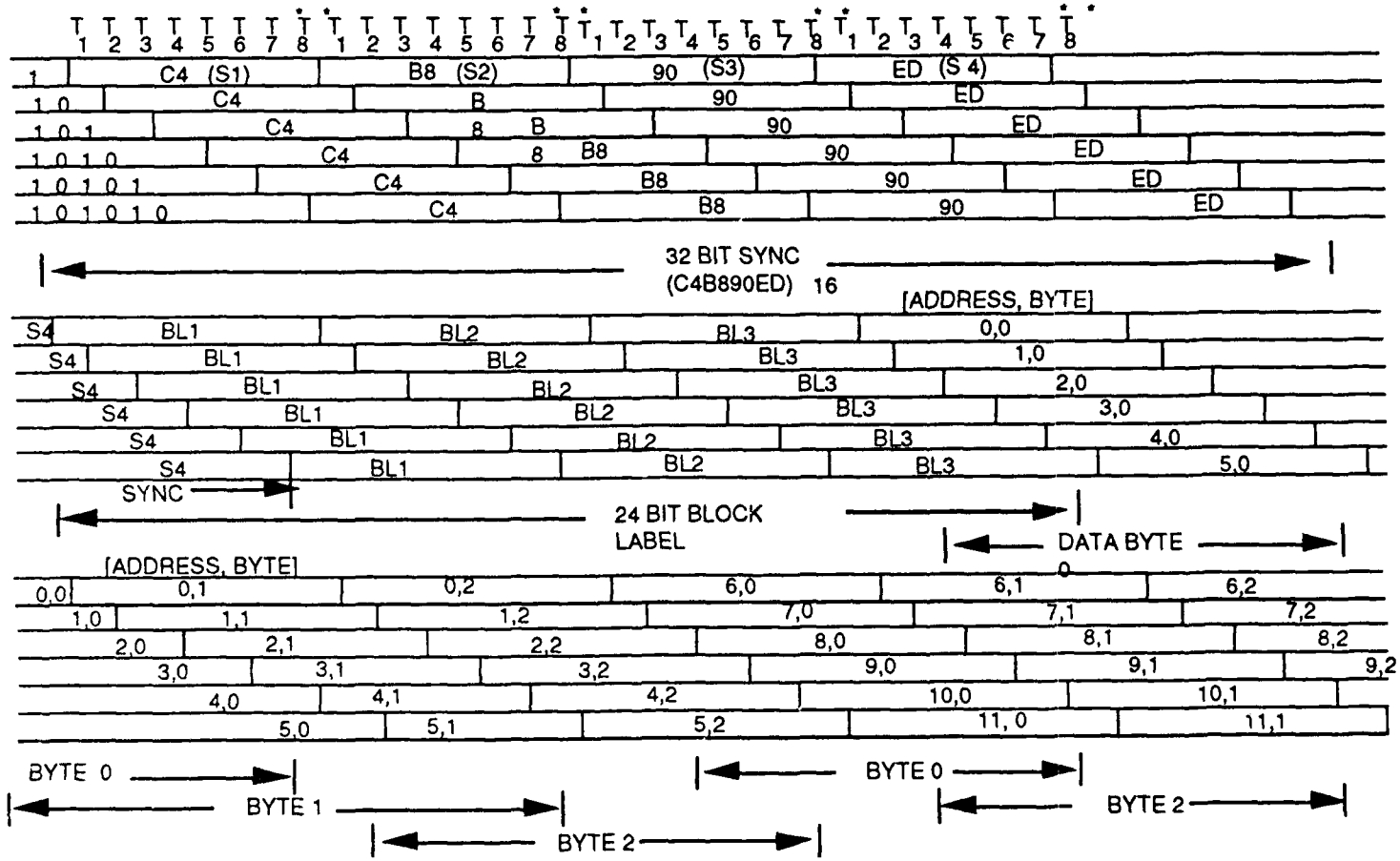

Figure 3-3. D-Bus Data Synchronization and Blocking

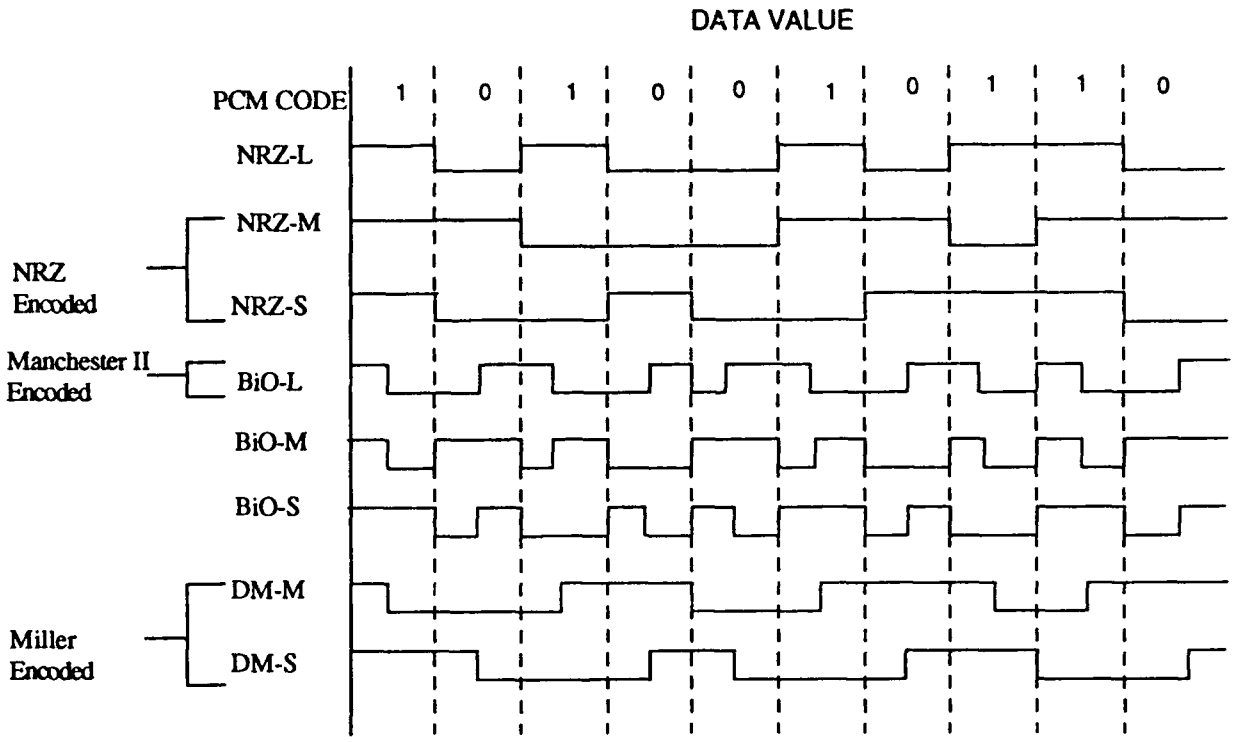

Figure 3-4. PCM Waveforms Diagram

3.2.1.2 PCM Codes

The following describes the pulse code modulation (PCM) codes utilized within the DICE system:

BIPhase-L [2]: A change in level occurs at the center of each bit period

"1" Is represented by a level during the first half of the bit period.
"0" Is represented by a level which is negative with respect to a "1" during the first half of the bit period.

DM-M [3]:

"1" Is represented by a level change at the center of the bit period.
"0" Is represented by another level change at the beginning of the bit period EXCEPT when the bit is preceded by a "1" in which case no level change occurs during the bit period.

---

2 BIPhase-L is also referred to as MANCHESTER II. It is the encoding scheme used by H-009 MUXBUS and the 1553 WEAPONS BUS.

3 DM-M is also referred to as MILLER CODE. It is the encoding scheme used by the HU as a direct input to the analog tape.

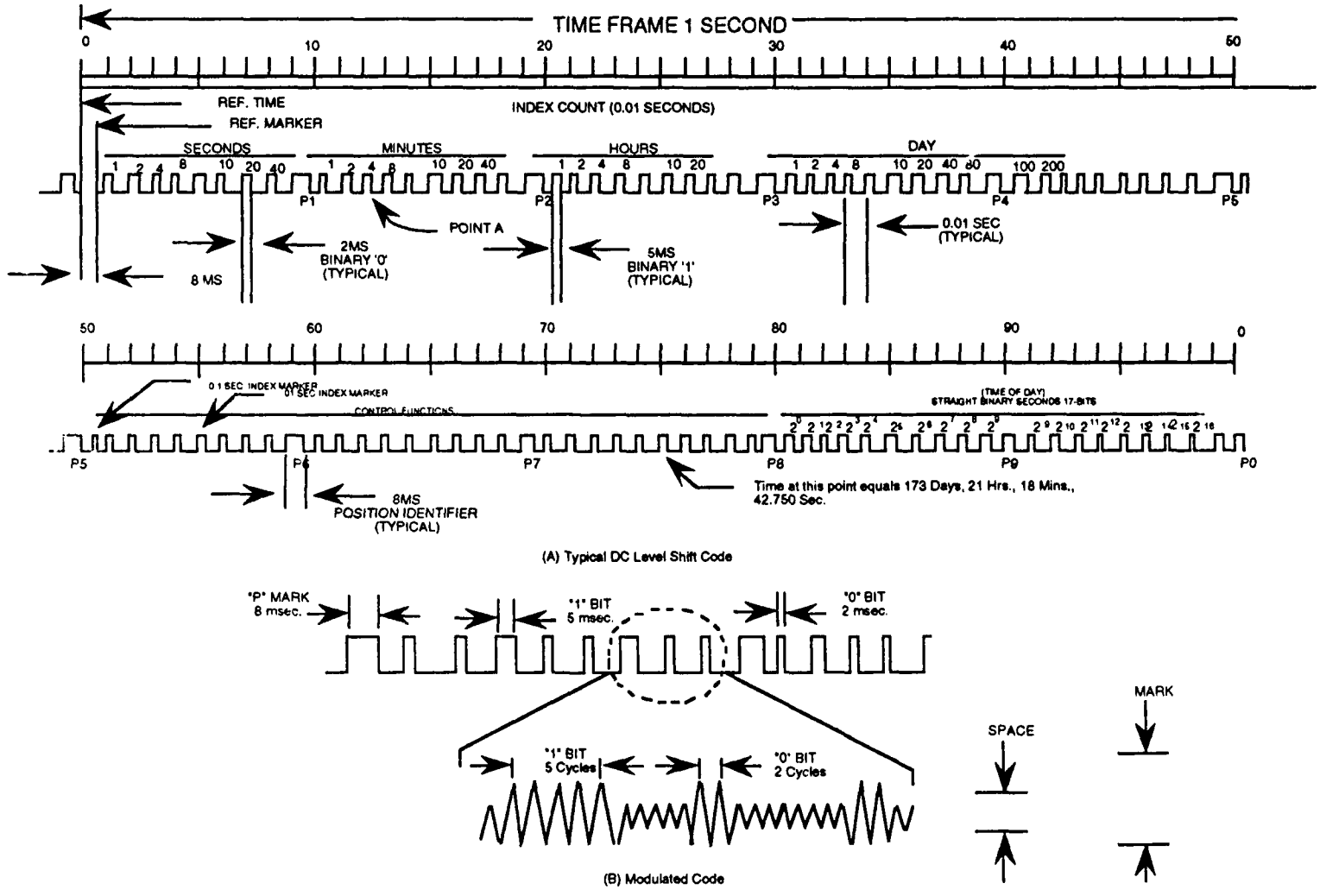

Figure 3-5. IRIG B Time Code Format

3.2.2 Mechanical Design

The mechanical design of the DICE laboratory prototype is an aggregate of the COTS devices. The custom designed hardware will be housed in the VME chassis.

Figure 3-6 represents the DICE system control box. The unit is a COTS VME chassis with five printed circuit board (PCB) slots. The I/O connectors to the laboratory IDRAS patch panel and the RS-423 operator terminal are located on the right side of the user space. The DICE system is configured as follows:

Slot 1:	VP1 Custom I/O control card
Slot 2:	RADSTONE CPU3A card
Slot 3:	Small Computer Serial Interface (SCSI) card
Slot 4:	MIL-STD-1553B Bus Monitor card
Slot 5:	Reserved for expansion

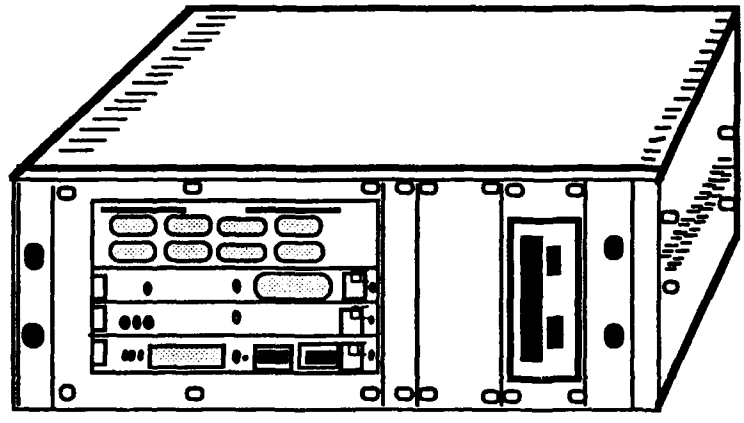

Figure 3-6. DICE System Control Box

Figure 3-7 gives the external dimension of the EXABYTE EXB-8500 tape cartridge system. This unit will be connected to the control box via cable to the SCSI controller.

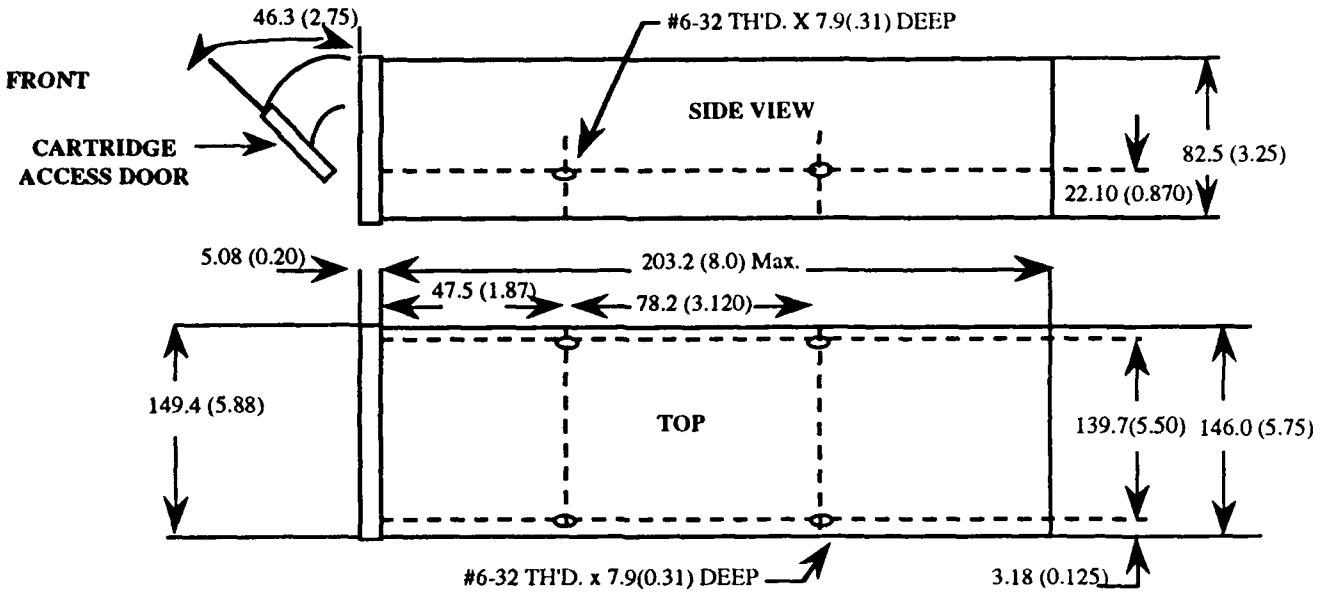

Figure 3-7. EXABYTE EXB-8500 Dimensions

Figure 3-8 represents the VP1 I/O development card which receives the data signals from the IDRAS patch panel, synchronizes with the words and messages, packs the data into 32 bit VME words, ID tags each VME word and interrupts the CPU for transfer via the VSB bus. The shaded area labeled "user area" is approximately 40 in^2. FPGA circuitry is used to execute the necessary configuration operations. The remaining portion of the PCB is populated with circuitry necessary to operate the VME communications and an 8 bit processor used to perform initialization and configuration.

3.2.3 Electrical Design

The complete schematic circuitry design for the VP1 I/O card is TBD for the draft ISD document. Figures 3-9 and 3-10 represent a portion of the VP1 card logic at a top level.

3.2.4 Data Source Pinouts

In the DICE laboratory demonstration system, the central computer multiplexer (CCMUX) connections signals have been converted to NRZ 0 to +5vdc. These signals are available at the IDRAS patch panel and will be accessed by using a BNC "T" connector at each signal cable patch point.

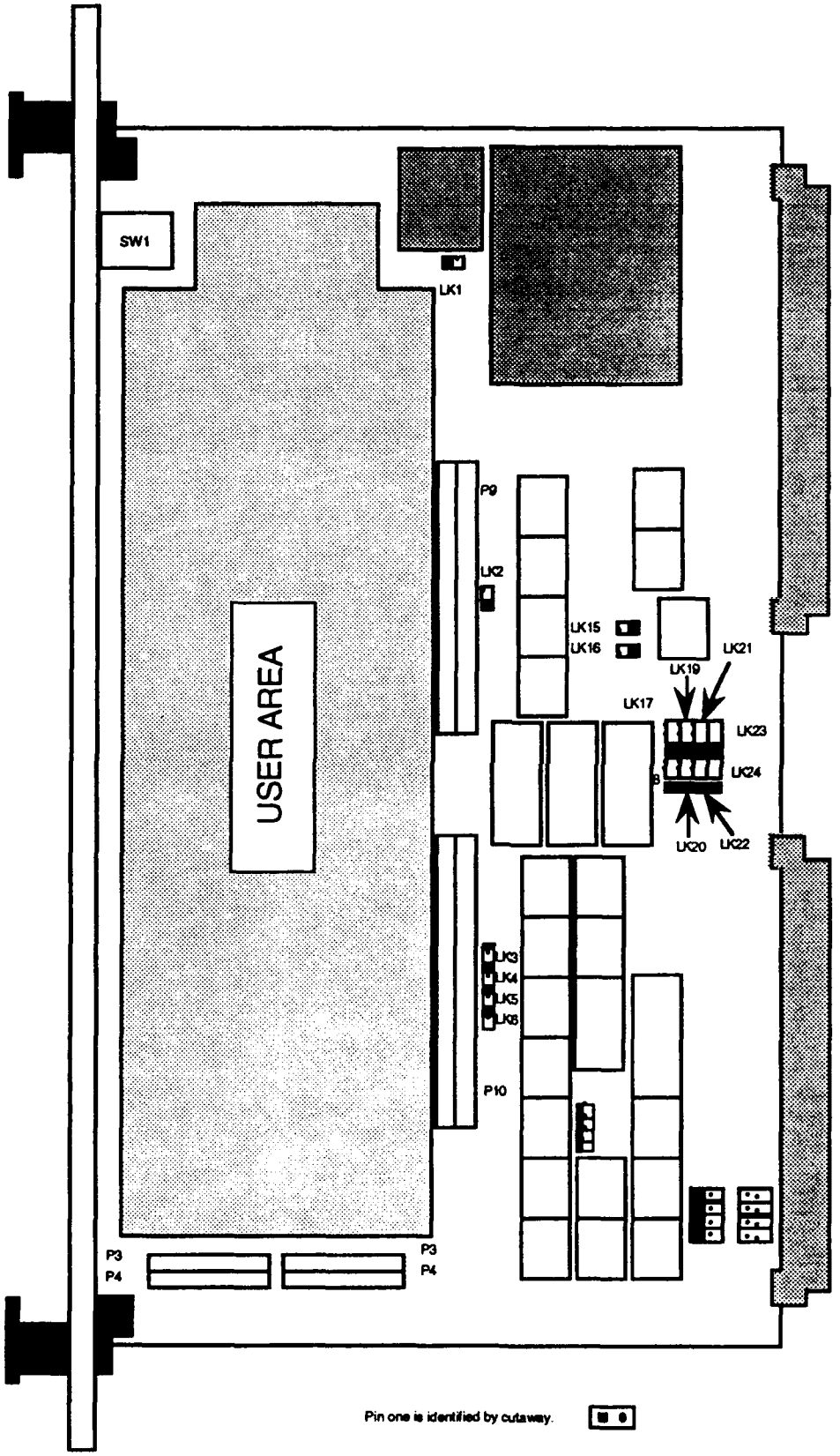

Figure 3-8. VP1 VME Development PCB

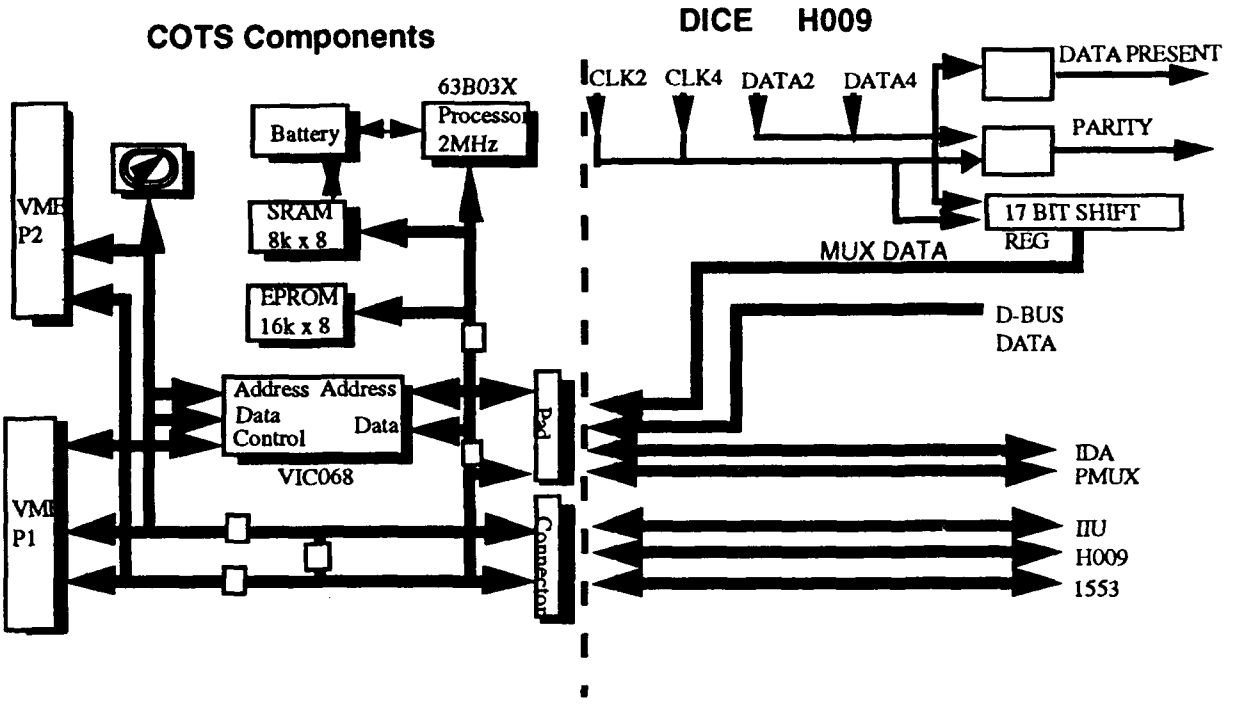

Figure 3-9. Top Level DICE H009 and IIU Interface Logic

3.2.5 Circuit Board Layout

3.2.6 EMI/EMC Considerations

The question of EMI/EMC effects and the DICE system is as yet unanswered. Under the basic DICE program, the laboratory prototype is unable to provide any insight in this area. Only with the flight worthy model can this issue be addressed. However, through careful selection of COTS components which have a low EMI/EMC characteristics for the laboratory prototype, the airborne version should subsequently have a low EMI/EMC profile.

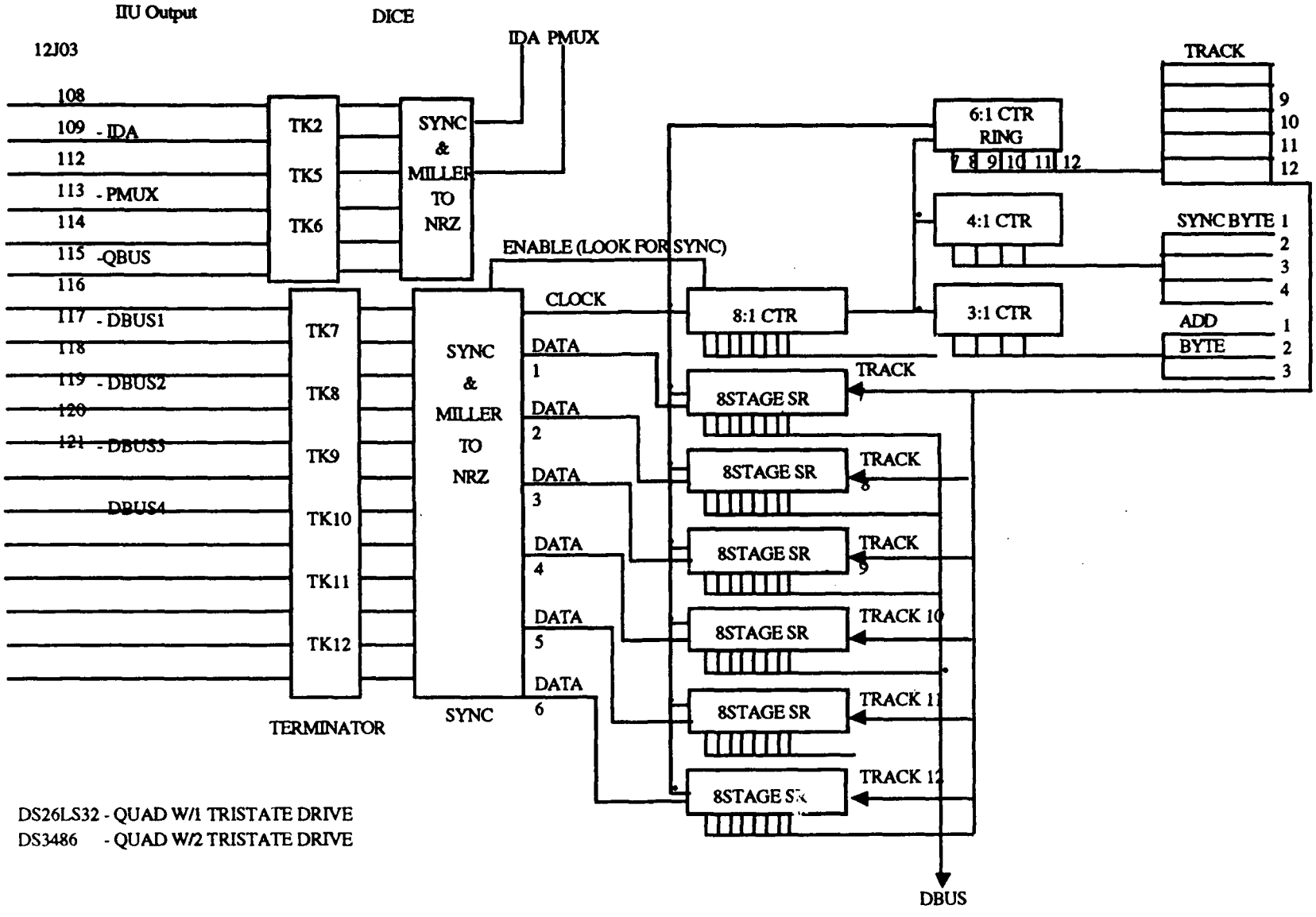

Figure 3-10. Detailed DICE H009 and IIU Interface Logic

3.3 Software Design

The DICE software configuration item (CSCI) consists of four computer software components (CSC). Each CSC is written in Ada. The CSCI is designed to perform both the data record and data replay functions of the DICE system. The DICE software is divided into two functional parts, the DICE Bootstrap Executive and the DICE System software (OFP - operational flight program). The DICE Bootstrap Executive is in firmware in the CPU3A card itself while the DICE OFP is downloaded from the EXABYTE tape system. This configuration allows for dynamic reconfiguration of the collection criteria and system configuration. The following paragraphs describe the function of each CSC. Figure 3-11 provides a top level view of the DICE software CSCI.

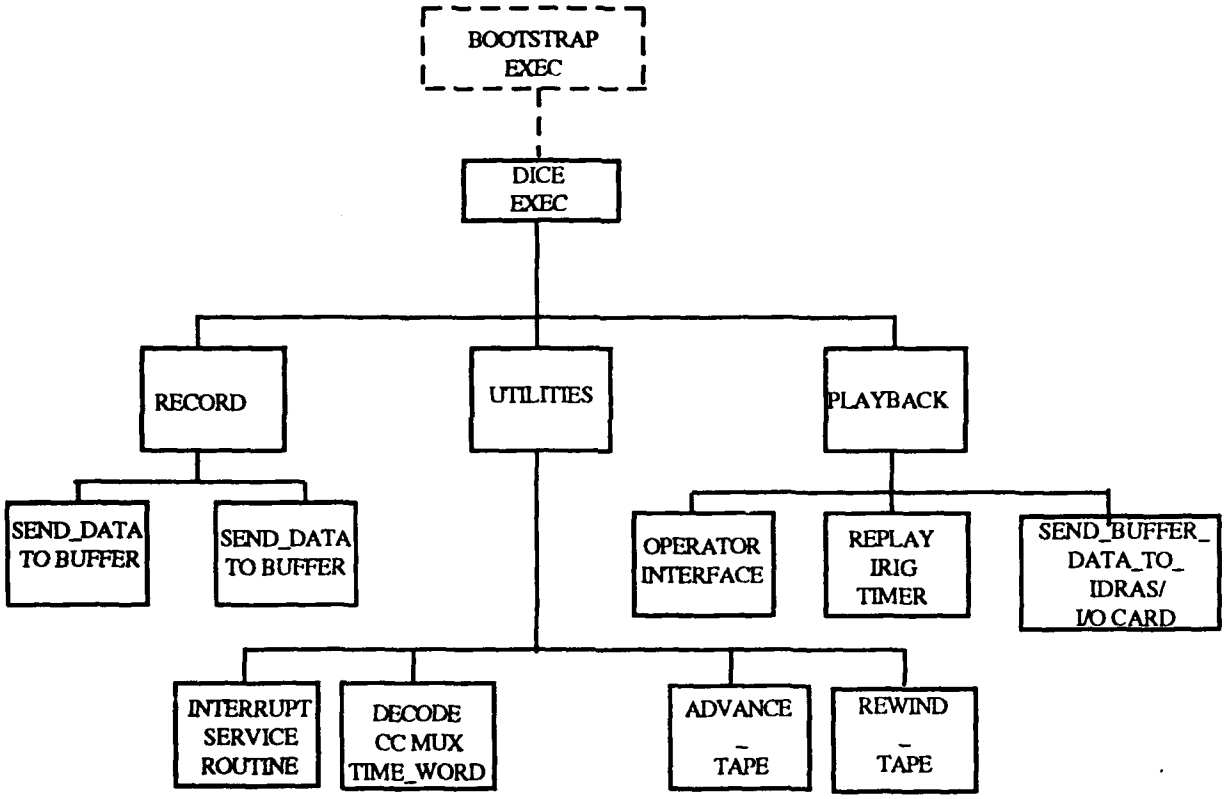

Figure 3-11. DICE CSCI Top Level Diagram

3.3.1 Bootstrap Executive

The Bootstrap Executive (BSX) CSC performs all of the necessary startup functions required to initiate the DICE system. The BSX is programmed into the user area of the CPU3A EPROM, where its functionality remains constant. At power up the Bootstrap Executive performs master processor built-in-test(BIT) and peripheral BIT. The BSX sets the appropriate status lights on the DICE control box when BIT results are negative. After successful startup, the BSX, utilizing the EXABYTE tape system, loads the DICE OFP into the CPU3A's RAM for execution. The BSX then transfers execution control to the DICE Executive CSC for operational functions. Figure 3-12 provides a state transition diagram for the DICE system.

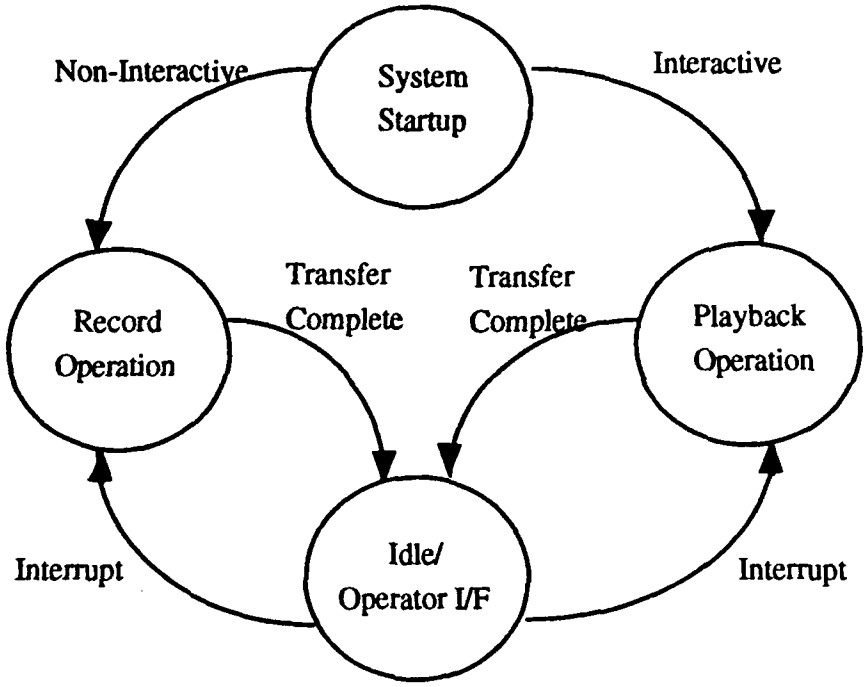

Figure 3-12. DICE State Diagram

3.3.2 DICE Executive

The DICE Executive (DEX) CSC provides control for the DICE system during operation. The DEX monitors all BIT reports and arbitrates control between the Record and Playback CSCs. The DEX determines the operational mode of the system and establishes the initial hardware configuration for the DICE system. Figure 3-13 depicts the processing flow of the DEX.

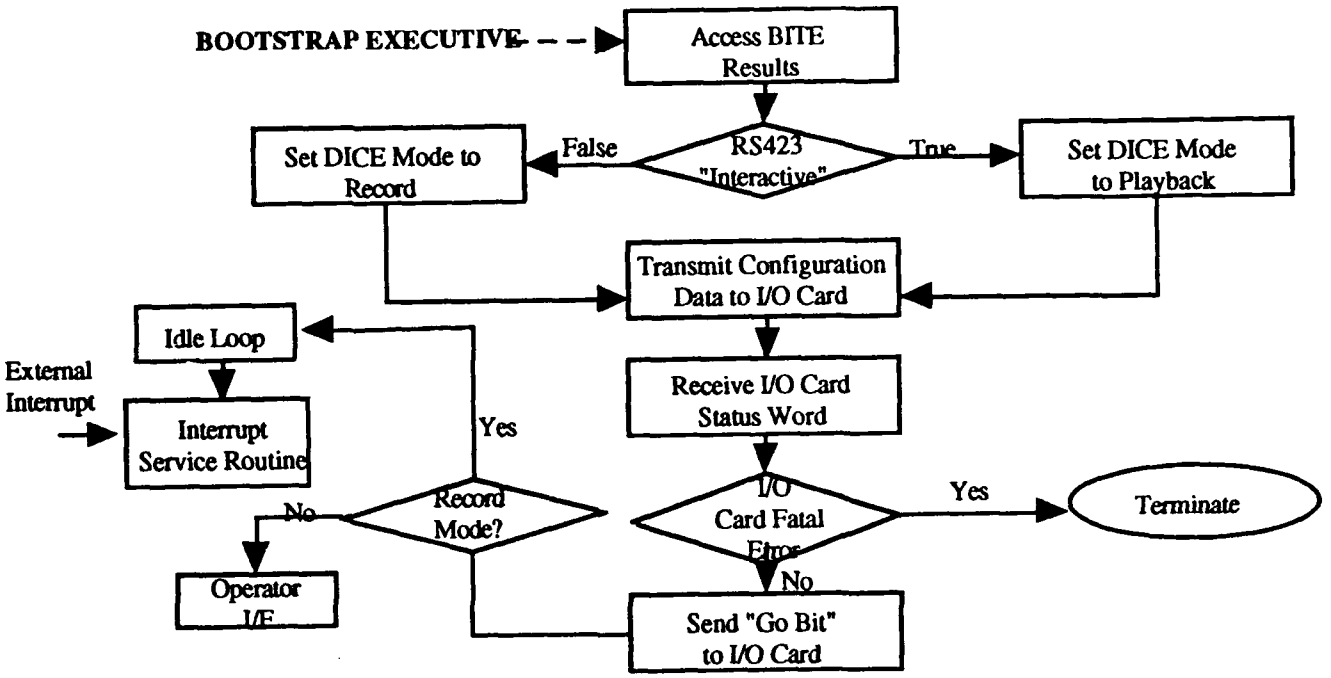

Figure 3-13. DICE Executive Processing Flow Diagram

3.3.3 DICE Record

The DICE Record CSC performs the data collection screening (Smart Record) and recording functions of the DICE system. DICE Record accepts the captured data from the VP1 I/O and 1553 monitor cards, and prepares it for storage on the EXABYTE tape system. Under the Smart Record option, the DICE Record CSC will perform criteria checks on the captured data to ensure that only the requested data is recorded. The DICE Record will also establish the control for reconfiguring the hardware, as necessary, for the Smart Record.

3.3.4 DICE Playback

The DICE Playback CSC performs the data playback function of the DICE system. DICE Playback accepts user specified start and stop times to control the transmission of recorded data. The DICE Playback provides the configuration control to setup the VP1 I/O 1553 monitor/control cards to transmit the data to the IDRAS patch panel.

3.3.5 DICE Playback

Table 3-2 provides the processing time and memory allocation budgets for the basic DICE system software (does not include Smart Record).

Table 3-2. DICE Software Timing and Memory Allocations

CSC/CSU/Data	Memory Budget (bytes)	Allocated Processing Time	Estimated Lines of Code
DICE Executive CSC	360	860 µSec	25
BIT CSU	240	240 µSec	20
Decode Time Word CSU	300	600 µSec	25
Operator Interface CSU	600	N/A	50
Advance Tape CSU	120	133000 mSec	10
Rewind Tape CSU	120	133000 mSec	10
Send Data Buffer CSU	300	0.0918 Sec	25
Receive Data Buffer CSU	300	0.0918 Sec	25
Bootstrap Executive CSC	600	720 µSec	50
Interrupt Service CSU	600	600 µSec	50
IRIG Timer CSU	600	600 µSec	50
Data Buffers	6144	N/A	N/A
Local Data	205	N/A	N/A

4 TEST PLANS

The following paragraphs describe the test methodology which will be used to ensure that the DICE system is functionally and operationally correct.

4.1 Hardware Test Plans

The DICE COTS hardware components will be tested for functionality based upon the advertised capabilities. Defects and departures from the stated capabilities will be noted and evaluated as to impact on the system design. The vendor will be challenged to explain and correct discrepancies prior to the component in question inclusion into the DICE system. If the vendor cannot correct a problem or demonstrate a work around, another source will be selected.

The DICE custom I/O card hardware configuration item (HWCI) will undergo three levels of testing to ensure functionality.

1) Logic Simulation testing. Utilizing CAD/CAE logic design tools, the designed circuitry logic will be simulated to test functionality of the design and correctness of components prior to being sent to PCB layout.

2) Board level testing. Using logic analyzers and other laboratory test equipment, the custom PCB will be tested for signals, rates, power, connectivity, and other crucial areas prior to hardware integration testing.

3) Integration Testing. Integration testing will consist of integrating the custom PCB and other hardware components to verify communications and control processing.

4.2 Software Test Plans

The DICE system software is to be developed in accordance with TRW's approved and accepted software development practices and procedures. The DICE CSCI will undergo five levels of testing and evaluation to ensure functionality and correctness.

1) Design Walkthroughs. The DICE CSCI design will be reviewed by the system engineer for functional, structural, and logical correctness prior to code and test.

2) Low Level Testing. Each low level software module or unit (CSU) will be tested during the code and unit test phase. Testing will consist of syntactical correctness, processing logic flows, data handling and exception handling.

3) Unit Level Testing. After each CSU of a CSC has passed unit level testing, the CSUs are integrated and tested. Testing consists of control flow checks, data communication, and functionality.

4) Control Testing. Each CSU/CSC which provides control for hardware within the DICE system is tested with the hardware for functionality. This testing is done in conjunction with the hardware engineer to resolve anomalies.

5) CSCI integration Testing. Each tested CSC is incorporated into the CSCI and tested for control flow and communications. Once this testing has been successfully completed, the CSCI is baselined.

4.3 System Integration Test Plans

After the DICE HWCI, COTS hardware and CSCI components have completed their respective testing, The system will be tested as a whole. System integration testing will utilize the advanced radar test bench system (ARTBS) located in the F-15 avionics integrated support facility (AISF) in Building 227 at Robins AFB GA. The integration test will be conducted as follows:

1) DICE system connected to the ARTBS through proper interfaces.

2) A known test scenario will be run on the ARTBS with both the DICE system and the laboratory recording device on. The test will be a minimum of five minutes.

3) The laboratory recorded data will be run through the IDRAS and a analysis report generated.

4) The DICE system will be configured to the replay mode and the recorded data transmitted to the IDRAS and an analysis report will be generated.

5) The two reports will be compared and anomalies identified and classified. The laboratory data is considered to be reliable and accurate.

These five steps will be repeated a minimum of six times (three test with one scenario, and three using a different known scenario). Any discrepancies will be reviewed and analyzed. Should changes be necessary to the DICE HWCI or CSCI, the changes will be submitted to a configuration control board (CCB) for review and evaluation. The CCB will consist of government and contractor personnel.

5 NOTES

5.1 Acronyms

AFLC	Air Force Logistics Command
AFSC	Air Force Systems Command
AISF	Avionics Integrated Support Facility
ARTBS	Advanced Radar Test Bench System
BSX	Bootstrap Executive
CCB	Configuration Control Board
CCMUX	Central Computer Multiplexer
COTS	Commercial-Off-The-Shelf
CSC	Computer Software Component
CSCI	Computer Software Configuration Item
CSU	Computer Software Unit
DEX	DICE Executive
DICE	Data Integration and Collection Environment
EMC	Electromagnetic Characteristics
EMI	Electromagnetic Interference
ESIP	Embedded Computer Resources Support Improvement Program
FPGA	Field Programmable Gate Array
HWCI	Hardware Configuration Item
IDRAS	Instrumentation Data Reduction and Analysis System
IIU	Instrumentation Interface Unit.
ISD	Instrumentation System Design
PACS	Programmable Armament Control System
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
MPRF	Medium Pulse Repetition Frequency
OFP	Operational Flight Program
SCSI	Small Computer Serial Interface
TBD	To Be Determined
TOR	Technical Operating Report

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